



A Fast Locking Duty Cycle Corrector(DCC) with High Accuracy

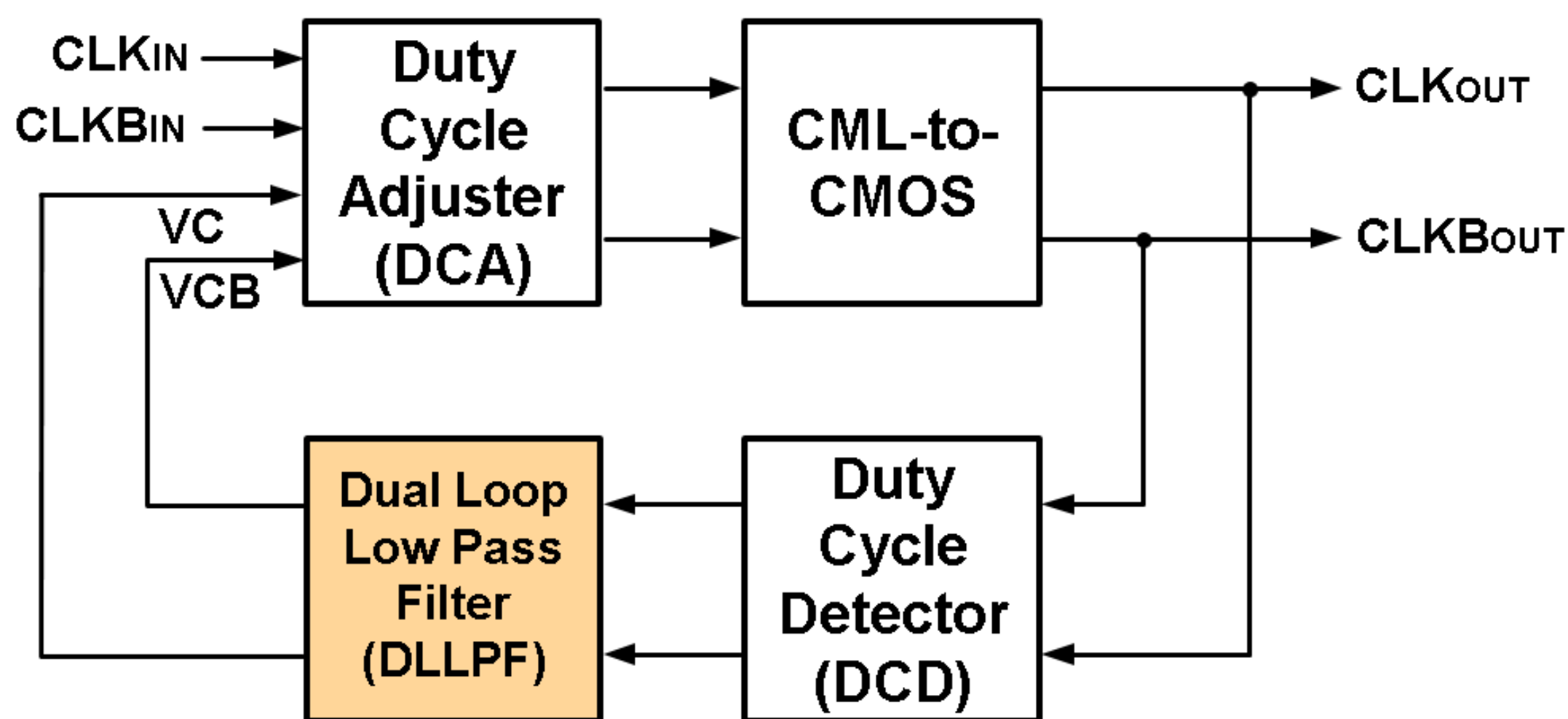
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Abstract

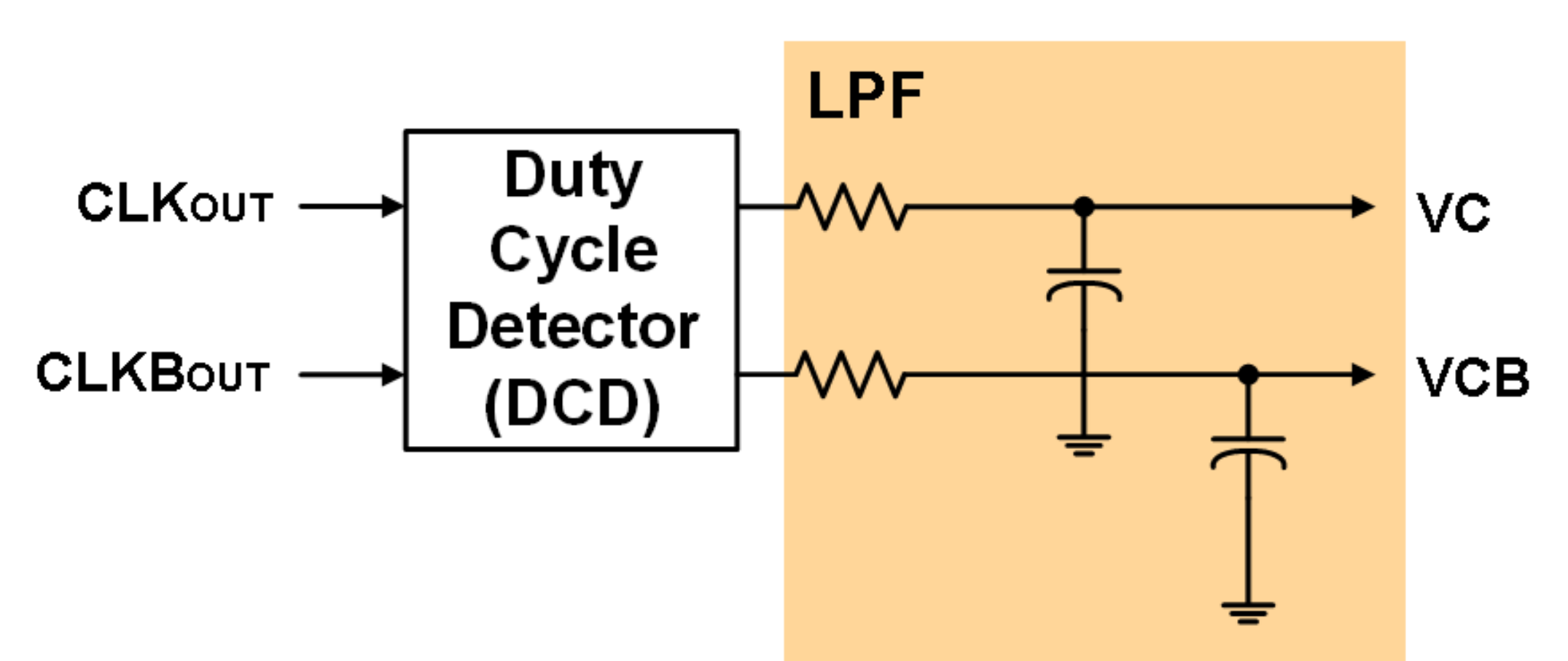
This poster proposes a fast locking duty cycle corrector with high accuracy for mobile memory. The proposed circuit has a dual loop low pass filter(DLLPF). The DLLPF has been proposed for high accuracy and fast correction time. The locking time is 1.89 times faster and the fluctuation is 9.21 times lower compared to conventional low pass filter. The output duty cycle is corrected to $50 \pm 1\%$ over the input duty cycle range of 20-80% for 1.6GHz. The circuit is implemented in CMOS 0.18- μm technology using 1.8-V supply.

Overall Structure of the DCC



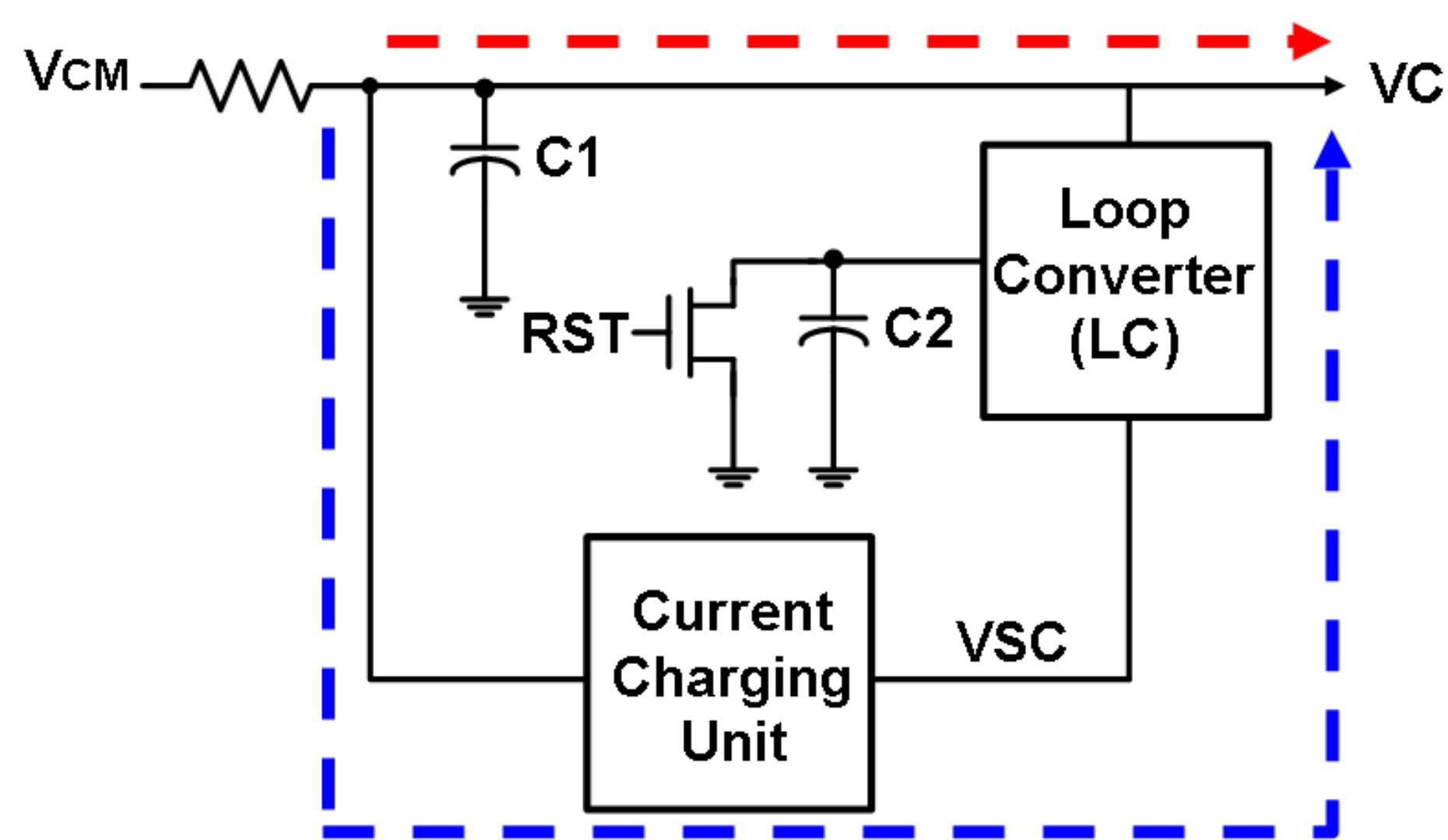
- DCD detects the difference between the average values of complementary CMOS clock signal CLKout and CLKBout.
- DLLPF converts the values detected by the DCD into offset voltages and transmits the voltages to DCA.
- DCA cancels common mode offset of input signal CLK_{IN} and CLKB_{IN} by receiving the voltages from the DCD and DLLPF.

Conventional LPF



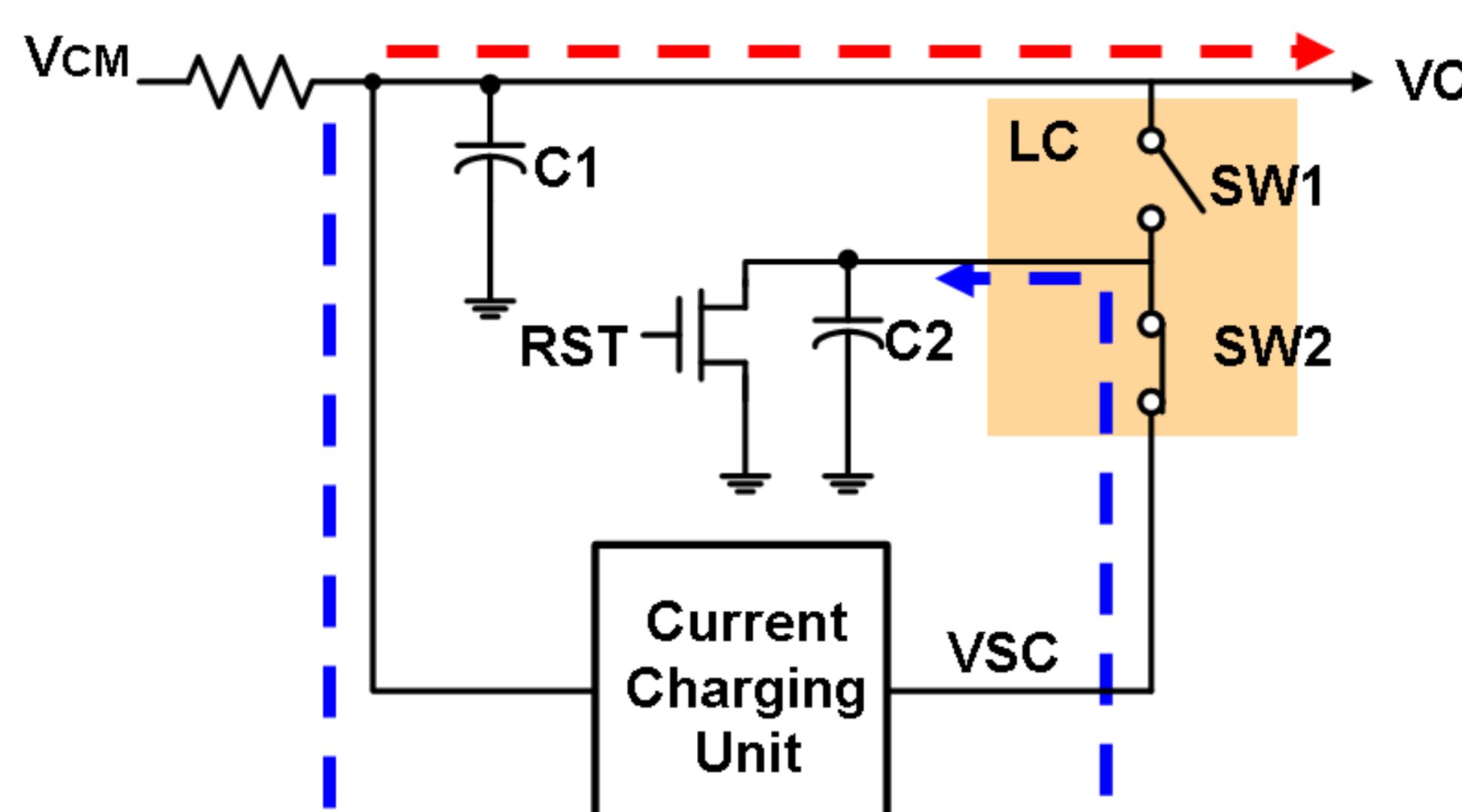
- Conventional low pass filter has a tradeoff between correction time and accuracy depending on its capacitor value.
- When the capacitor value is small, it has a wide bandwidth and fast correction time, but noise increases and accuracy is poor.
- When the capacitor value is large, it has a narrow bandwidth and slow correction time, but the noise is small and accuracy is good.

Proposed DLLPF



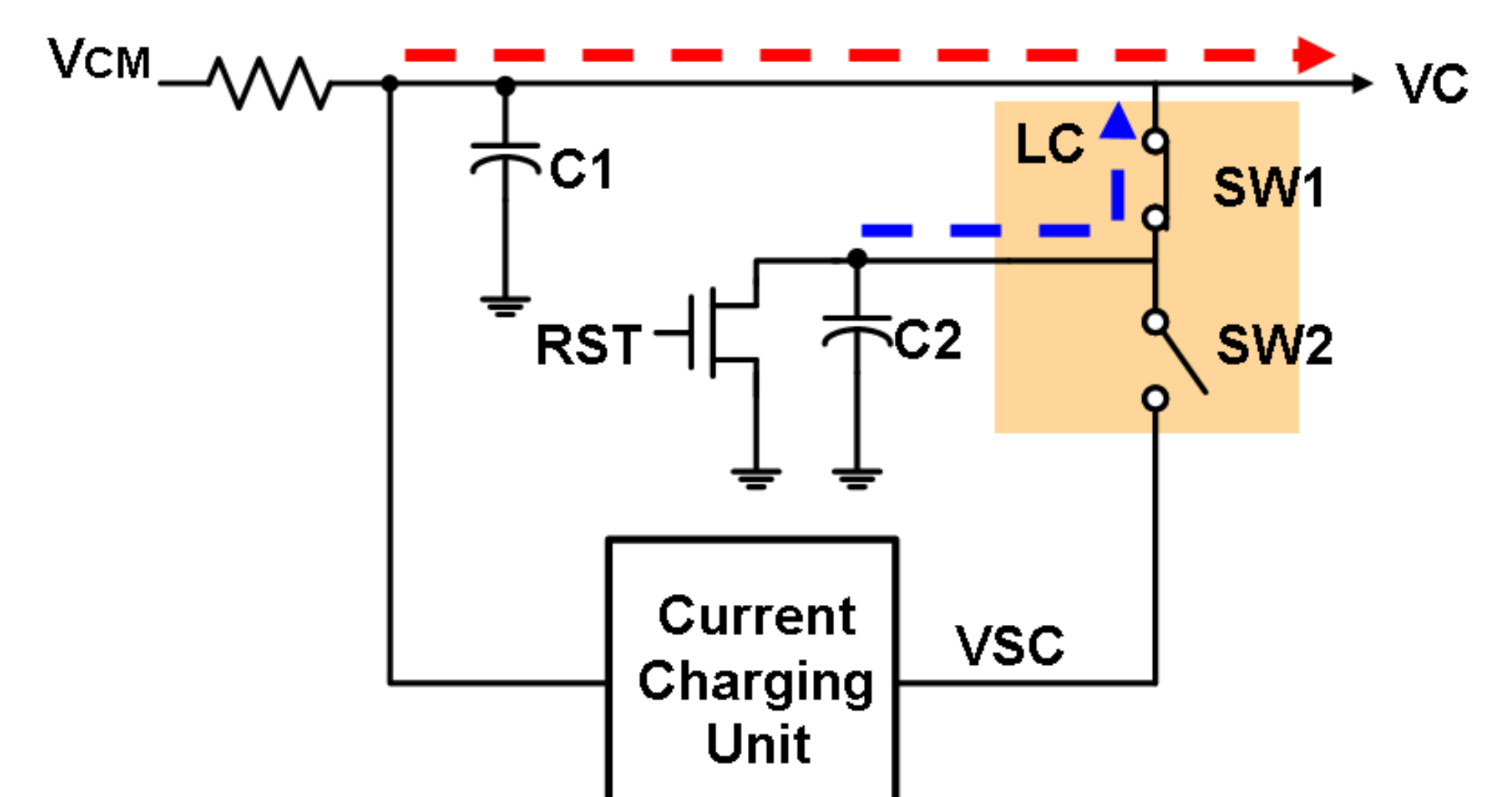
— : Main Loop
- - : Sub Loop
C1 : 100fF
C2 : 3pF
< Dual Loop Low Pass Filter >

< Operation of DLLPF① >



- The DCC is operated using the Main Loop.
- C2 is charged by Current Charging Unit in the Sub Loop quickly.

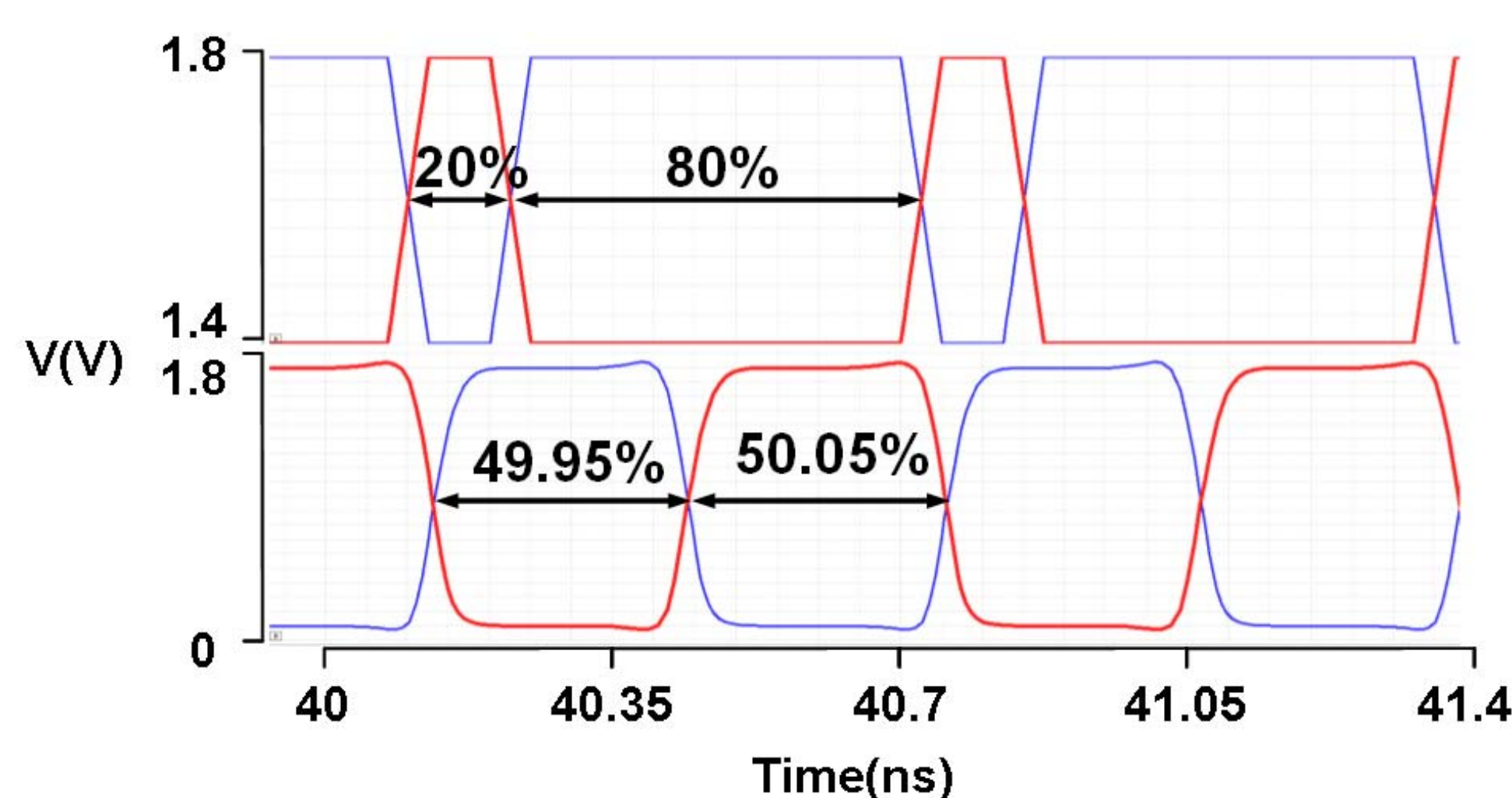
< Operation of DLLPF② >



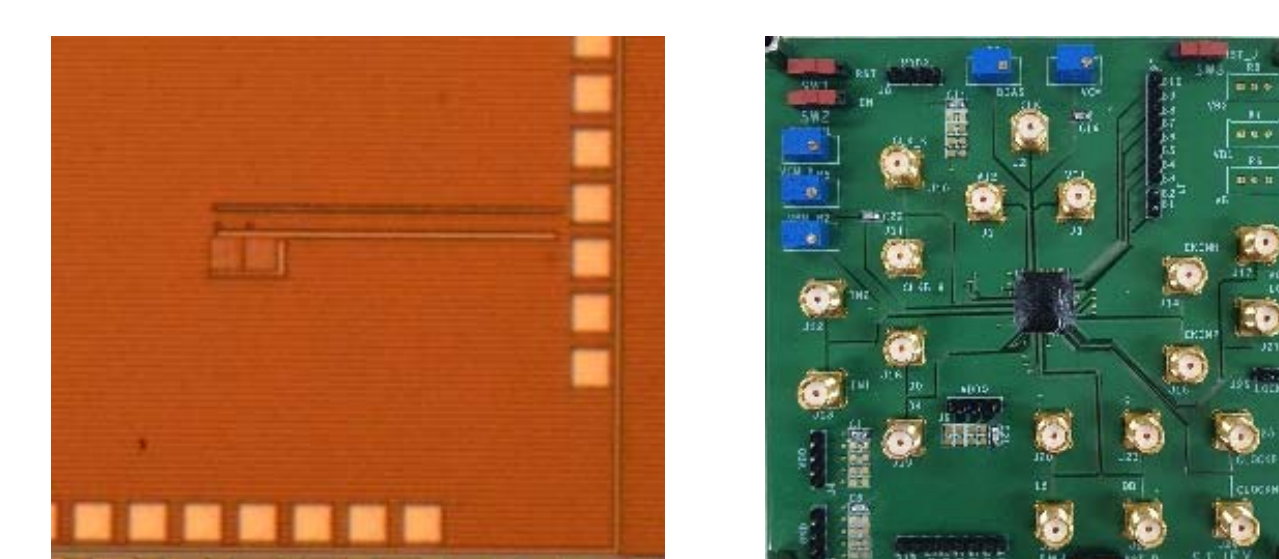
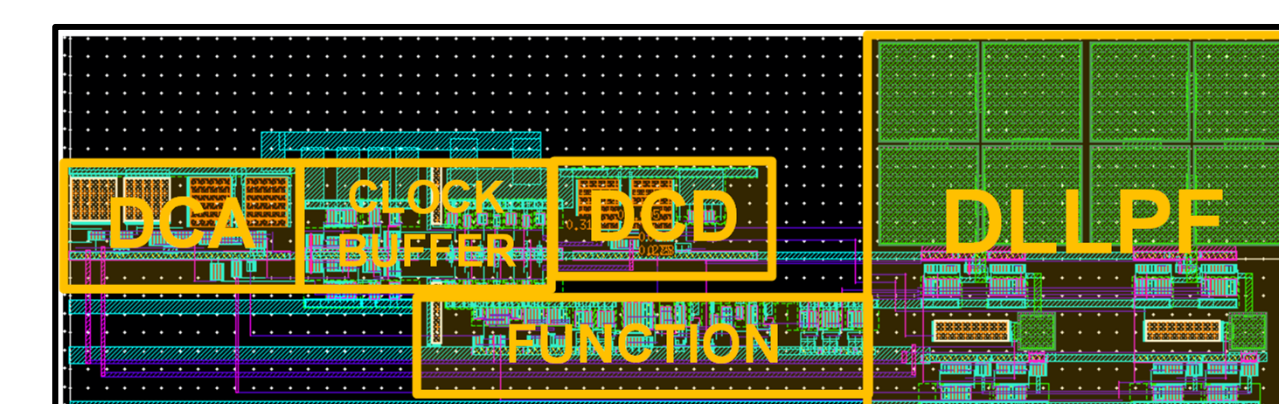
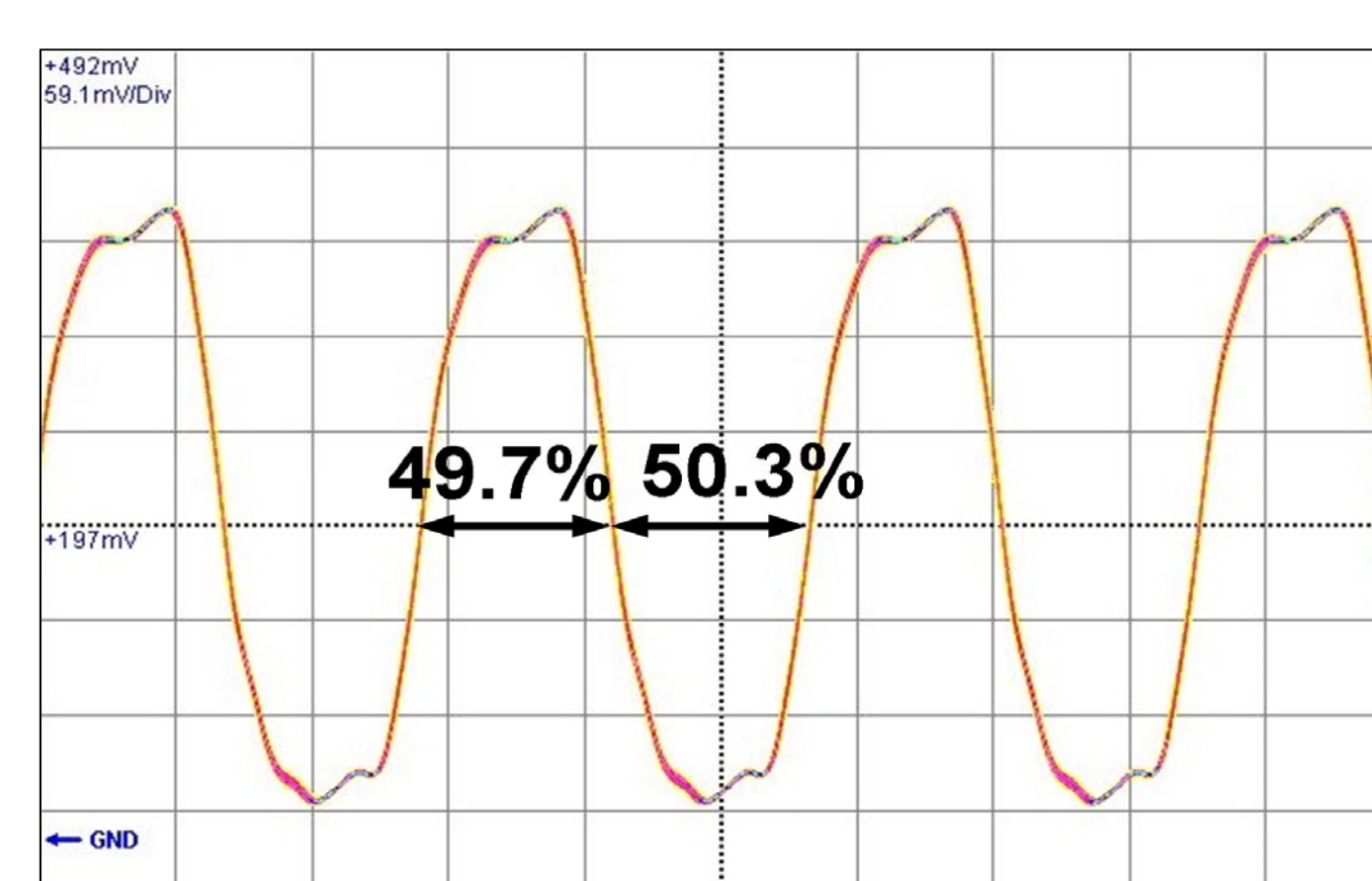
- The DCC is locked by the main Loop.
- If VC = VSC, LC is switched by signal from Comparator.

Experiment Results

Post-simulation result of the proposed DCC for duty cycle distortion of 20% at 1.6GHz.



Measurement result of the proposed DCC for duty cycle distortion of 37.5% at 1.56GHz.



Layout, Microphotograph and PCB of the proposed DCC

Summary Table

Process	CMOS 0.18um
Supply Voltage	1.8V
Clock Freq.	1.6GHz
Jitter	15.04ps
Power Consumption	31mW

Conclusion

- A duty cycle corrector using dual loop low pas filter can obtain both fast locking time and high accuracy.
- In post-simulation result, the locking time is 1.89 times faster and the voltage fluctuation is reduced 9.21 times compared to the conventional low pass filter.

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